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Power Conversion for UHVDC to UHVAC Based on Using MMC with Large Scale of Output Voltage Level

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Abstract: **Ultra-high voltage DC (UHVDC) transmission systems are among the most promising systems to transmit power for distances up to 3000 km and ultra-voltage up to 2200 KVDC. One of the most challenging issues associated with UHVDC is the conversion of power at the receiving end of UHVDC transmission systems. This paper proposes a pulse-width modulation (PWM) algorithm based on flooring technique for modular multilevel converters (MMCs) to be used with a large scale of submodules per arm that can convert UHVDC 2200 KV and more to UHVAC, reducing total harmonics distortion (THD) for UHVAC less than 1%. A literature review concerns MMC topology and control. Generating insertion indices for number of submodule per arm (N) is derived first. Second, flooring switching PWM is explained to generate number of inserted and bypassed submodules per arm. Third, analysis of the balancing of the submodules voltages and submodules selection, the key technique to achieve insertion and equalization between arm submodules, is proposed and verified by simulation and experiment. Fourth, a set of simulation results for DC bus 2200 KV and 481- level for the output voltage conducted in MATLAB/Simulink environment verify the proposed algorithm. Finally, the prototype's hardware design and software design verify the proposed PWM algorithm experimentally. This paper shows the experimental results.**

Keywords: **Modular Multilevel Converter, MMC with Large Number of Submodules.**

I. INTRODUCTION

MMC had been invented by Lesnicar and Marquardt as a development from the Cascaded H-Bridge Converter [1]. MMC was first presented as AC to AC and DC to AC converters, for high-power experimental prototypes [6]. MMC was presented as a cascaded converter based on cascading identical submodules [7]. The selection submodules have to be inserted or bypassed for each arm of the converter while maintaining each submodule capacitor voltage around its reference voltage, and phase arm modulation is an important aspect in the operation of the converter. The submodule, the heart of a MMC, has had its operation and circuit configuration explained before [1], [2], and [12]. [12] simplifies the MMC by considering the sum of capacitors voltages in each arm instead of individual capacitor voltage. A number of papers discussed modulation methods based on multilevel SPWM for MMC topology in the technical literature [13], [15]. The modeling of nonlinear control of MMC was introduced in [19]. PWM for a limited number of voltage levels was presented in [21], which used average PWM pattern over a switching period to determine switching of MMC. [23] described the number of connected or bypassed submodules by direct modulation for small number of submodule per arm based on the floor value between the reference sinusoidal signal and the number of submodules for each arm. Optimizing MMC patterns has also been a subject of research, with [24] studying MMC under selective harmonic elimination PWM and a fundamental frequency switching pattern as in [25]. Different control approaches with various modulations were presented in [4], [25] and [26] to investigate dynamic and required voltage balance of MMC topology. A number of applications such as voltage source converter-based HVDC transmission, STATCOM, and back-to-back converter had been studied based on the use of MMC [3], and [27]. Also, in [28] and [29], high-voltage super-grids provided the possibility of using MMC in the configuration for multi-terminal HVDC. The modular topologies classification, presented in [7], does not rate the converter as a topology with many useful submodules for a DC system that can transmit up to 2200 KV. Power losses for both the converter and its submodules were evaluated in [5], and [30]. In [31], submodules

losses were evaluated by utilizing different configurations for MMC. The effect of sampling frequency on THD in the operation of the converter was analyzed in [32]. Also, the effect of dead time in the submodule of the converter was considered in [33]. [34] presented minimization method of DC-link ripple, mathematical model for the capacitor voltage variations, and improved voltage balancing control system for MMC in the converter topology [35]. Arm inductance and submodule capacitance can be calculated in different methods as in [37], [38], and [39]. Also, smoothing reactor for HVDC systems has been evaluated exactly [40] and approximated [41]. Transmitting power 10,000 MW and distance up to 3000 km with ± 1100 kV DC is consider economic, efficient, mature technology [6] and [42]. The DC bus voltage of UHVDC transmission system determines the number of submodules per arm. Therefore, with 2200 KVDC ([6], [42], [43]), each converter arm consists of a large number of submodules.

II. OPERATION PRINCIPLES AND CONVERTER EQUATIONS

Figure1 illustrates a final single-phase MMC circuit with its submodule. Since the capacitors are not guaranteed to provide constant voltage when connected to a circuit, this brings some problems. If a capacitor is inserted in the arm, its voltage varies according to the direction of the current. The simplest and accurate solution is to use the effect that charges and discharges the capacitors actively in the converter modulation itself through a specific algorithm will be explained in detail later in this paper. However, capacitor voltages are still inconstant, something which could cause current transience due to unequal voltages between the legs. For this reason inductances are also placed in each arm. The heart of the MMC is the submodule and its basic half-bridge scheme appears in Figure1.

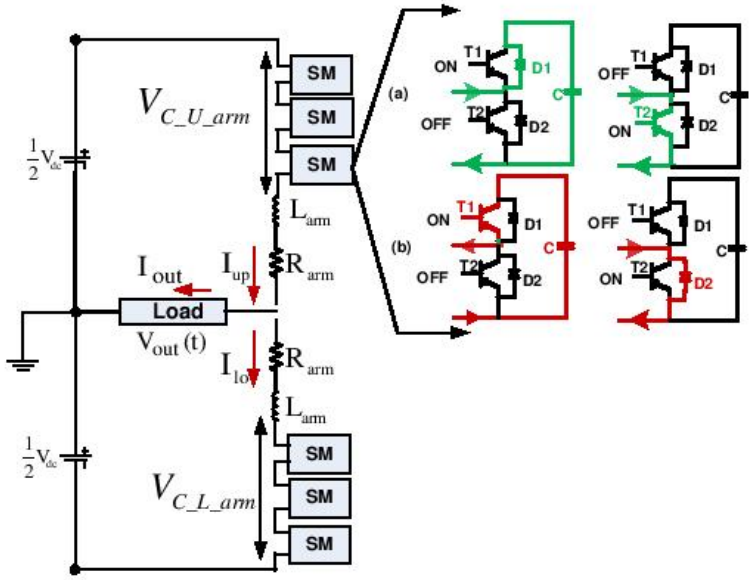

Figure 1. Single-phase MMC circuit and its submodule ((a) Positive and (b) negative current flow inside a MMC submodule

To explain how the proposed PWM algorithm works for MMC circuit, a specific example will show how to generate a voltage waveform. In this example, the number of submodules per each leg will be 4; the converter will convert DC to AC with 5-level waveform (n=N+1; where n number of output voltage level), which will be explained in details. The voltage across each capacitor can be given as in (1):

TABLE I. SWITCHING STATES FOR EACH SUBMODULE

T1	T2	D1	D2	Current direction	Capacitor state	Output voltage
OFF	ON	OFF	OFF	$I_{arm}>0$	Uncharged (bypassed)	0
OFF	OFF	OFF	ON	$I_{arm}<0$	Uncharged (bypassed)	0
OFF	OF	ON	OF	$I_{arm}>0$	Charging	V_C

	F		F			
ON	OFF	OFF	OFF	$I_{arm}<0$	Discharging	V_C

$$V_C = \frac{V_{dc}}{N} = \frac{V_{dc}}{4}\ V. \qquad (1)$$

V_{dc} is DC bus voltage, and assuming the submodule selection process is effective, the submodule capacitors within a converter arm can be assumed to be equally charged. This is possible with a switching frequency high enough to allow the modulator to act even on very small disturbances in this balance. It will be proven later that these assumptions can apply for a small number of submodules. Figure1 shows an equivalent electrical circuit for one phase leg of MMC and Table II shows MMC parameters definitions. Let the converter consist of N submodules per arm. In general, each arm is controlled by an insertion index x, which is defined such that x = 0 means that all N submodules in the arm are bypassed, while x = 1 means that all N submodules in the arm are inserted. Table I shows switching status for all submodule component. In the former case, the current is flowing through the arm will not pass through any capacitor, so the equivalent capacitive arm impedance is zero. In the latter case, the arm current will meet N capacitors connected in series, making the equivalent capacitance of the arm C/N. If each submodule capacitor has capacitance C, the effective capacitance of the one arm is given by (2):

TABLE II. MMC PARAMETER DEFINITIONS

C	Submodule capacitance
x	Insertion index
I_{up}	Upper arm current
I_{lo}	Lower arm current
I_{cir}	Circulating current
I_L	Output phase current
x_U	Insertion indices of the upper arm
x_L	Insertion indices of the lower arm
$V_{C\_U\_arm}(t)$	Total upper arm capacitor
$V_{C\_L\_arm}(t)$	Total lower arm capacitor
V_{dc}	DC bus
V_{out}	Output phase voltage

$$C_{arm} = \frac{C}{N.x}\ . \qquad (2)$$

Naming the upper and lower arm currents I_{up} and I_{lo} respectively, and defining their polarities as illustrated on Figure1, the output phase current is calculated as their sum in (3).

$$I_L = I_{up} - I_{lo}. \qquad (3)$$

The output phase current is assumed to be equally shared by both upper and lower arm. However, and as mentioned in previous paragraphs, there is a deviation from this ideal condition since part of the current passes through the series-connected arms and the DC source. Let this circulating current be called I_{cir} as in (4).

$$\left.\begin{aligned} I_{up} &= I_{cir} + \frac{I_L}{2} \\ I_{lo} &= I_{cir} - \frac{I_L}{2} \end{aligned}\right\} \xrightarrow{\sum} I_{cir} = \frac{I_{up} + I_{lo}}{2}. \qquad (4)$$

In a three-phase system, $I_{cir} = \frac{1}{3} I_{dc}$ and in a single phase system, $I_{cir} = I_{dc}$, where I_{dc} is DC source current.

Defining x_U and x_L as the insertion indices of the upper and the lower arm respectively, the following equation is derived:

$$V_{out} = \frac{x_L V_{C\_L\_arm} - x_U V_{C\_U\_arm}}{2} - \frac{R_{arm}}{2} I_L - \frac{L_{arm}}{2} \frac{dI_L}{dt} \quad (5)$$

Where V_{out} the output phase voltage, by solving the last two equations, the equivalent voltage for the external load connected to the AC terminal becomes, and $V_{C\_U\_arm}(t)$ and $V_{C\_L\_arm}(t)$ are total upper arm capacitor voltage and total lower arm capacitor respectively.

III. PROPOSED PWM ALGORITHM

Figure2 shows the general flowchart for the proposed PWM algorithm with its steps which they will be explained as follow:

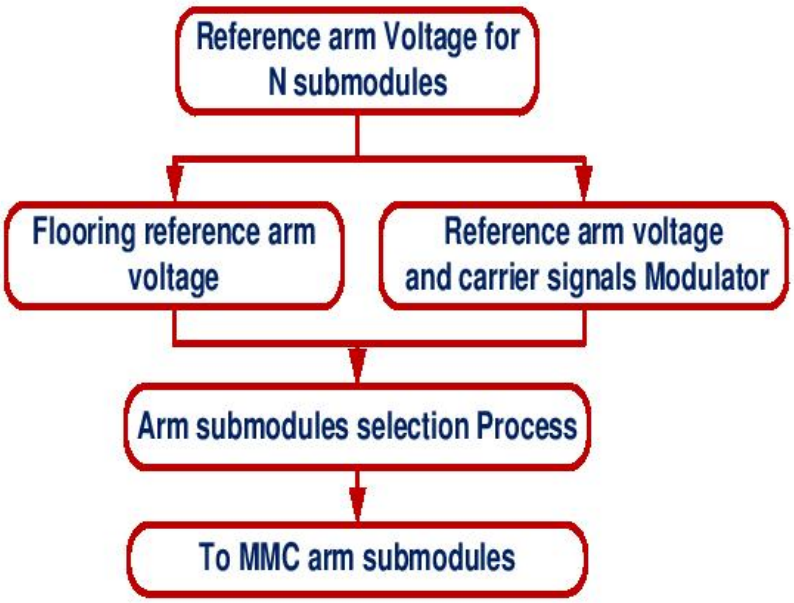

Figure2. Proposed PWM algorithm flowchart

1. Reference arm voltage for N submodules

The proposed PWM algorithm of MMC is based on the equalization of the inserted submodules for one arm with the bypassed submodules for the other arm. First, the operation of MMC as n (N+1) level converter is discussed. The principle is that in each instant, N submodules are inserted and N submodules bypassed for the whole leg. Let N_U be the number of submodules inserted in the upper arm and N_L the number of submodules inserted in the lower arm. Accordingly, the AC terminal can take N+1 different potentials when the number of inserted modules varies between 0 and N. A sinusoidal reference is applied to the modulator, which is then converted into a varying insertion index for each arm as defined by (6), where ω_N is the angular frequency of the output voltage.

$$m(t) = N * \hat{m} \cos(\omega_N t) \quad (6)$$

$\hat{m}$ is the maximum value for modulation index, which is 1. The main target from this process getting number of inserted submodules for both arms with keeping the condition of this method mentioned above. Therefore, equation (6) will split into two equations (7), leading to (8) and (9):

$$\left.\begin{aligned} N_{U,bypassed} &= N - N_{L,bypassed} = N_{L,inserted} \\ N_{U,inserted} &= N - N_{L,inserted} = N_{L,bypassed} \end{aligned}\right\} \longrightarrow \quad (7)$$

$$N_U = \frac{N - N * m(t)}{2} \qquad (0 < N_U \leq N) \quad (8)$$

$$N_L = \frac{N + N * m(t)}{2} \qquad (0 < N_L \leq N) \quad (9)$$

This step is considered a starting point for indirect PWM as can be seen later. Figure3 shows m(t) and number of inserted submodules for both upper and lower arms in sinusoidal waveform.

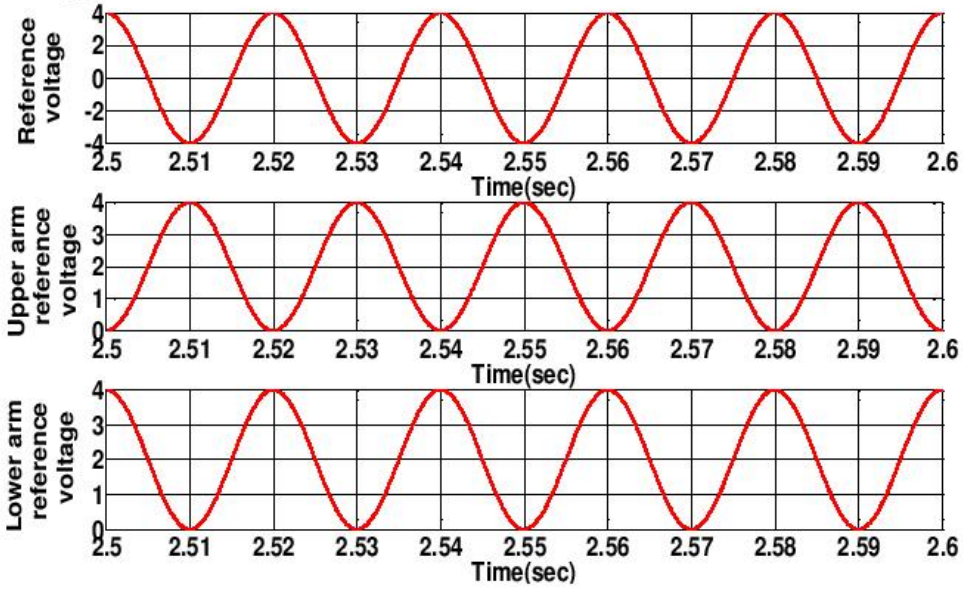

Figure 3. Reference voltage, number of inserted submodules for both arms in continuous mode

2. Flooring arm reference voltage

Because the numbers of inserted or bypassed submodules for both arms are real, positive, and integers, flooring of both sin waves of upper and lower arms must be done for this purpose. Flooring value (a) is choosing (a) to the nearest integer in the direction of negative infinity, while ceiling value (a) is choosing (a) to the nearest integer in the direction of positive infinity. For example, the flooring value for 0.5 is 0 and the flooring value for 1.99 is 1. Figure4 shows the number of inserted submodules for both arms after flooring (green signal is N before flooring and blue signal is N after flooring).

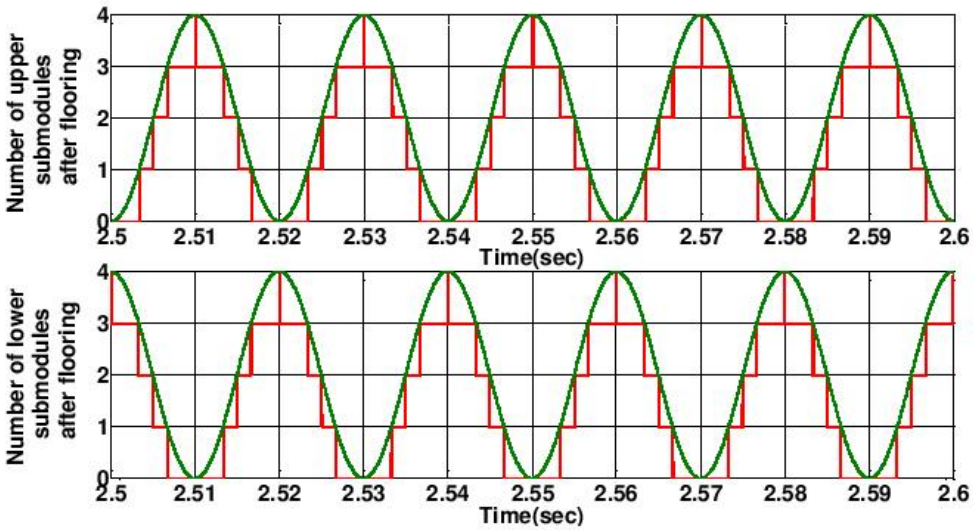

Figure4. Number of upper and lower submodules after flooring.

3. Reference arm voltage and carrier signals modulator

At the same time as the last step, the modulation process of the reference signals for both upper and lower arms with carrier signal, which has a switching frequency for the switches and can be seen in Figure5, is done. The modulator will modulate both signals to the waveform in Figure6 for both upper and lower arms, respectively, in a process which aims to create a signal which matches an assigned reference by averaging the number of inserted submodules between a floor and a ceil number in every sampling period. This process determines the inserted submodules for both upper and lower arms and the exact instants of the switching actions. Figure6 shows both inserted submodules for upper and lower arms at the same time; it is obvious that the number of inserted submodules in one arm is equal to the number of bypassed

submodules in the other arm, which achieves the balancing voltages between upper arm and lower arm across the AC terminal. As described in the previous paragraphs, MMC output and circulating currents are determined by the state of the submodules within the arms of the converter. The voltage determining the output current of the converter is derived by the variation of the submodules' voltages connected to the upper and lower arms.

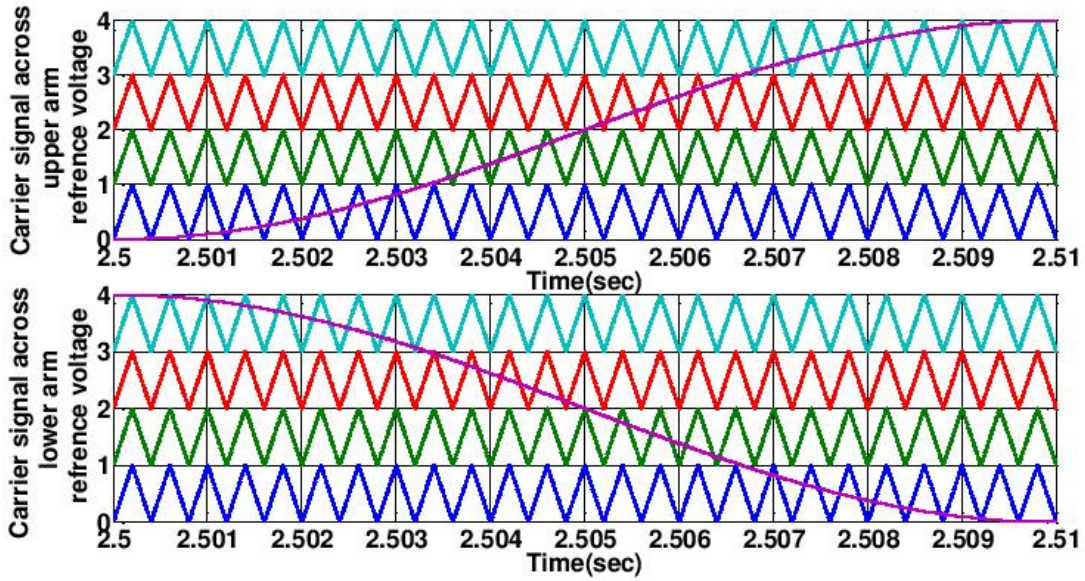

Figure 5. The reference signals for both upper and lower arms across carrier signal.

A sinusoidal waveform in the output can therefore be achieved by varying the number of the submodules in the upper and lower arms in a sinusoidal manner. Because the voltage of each arm is not continuous but varies based on the switching of the submodules, the selection of the submodules and the PWM method applied to the converter affect its operation and output waveforms. The two arms that comprise the phase leg of the converter can be modulated either simultaneously or independently of each other. The number of submodules to insert or bypass was found by comparing the voltage reference with carrier waves.

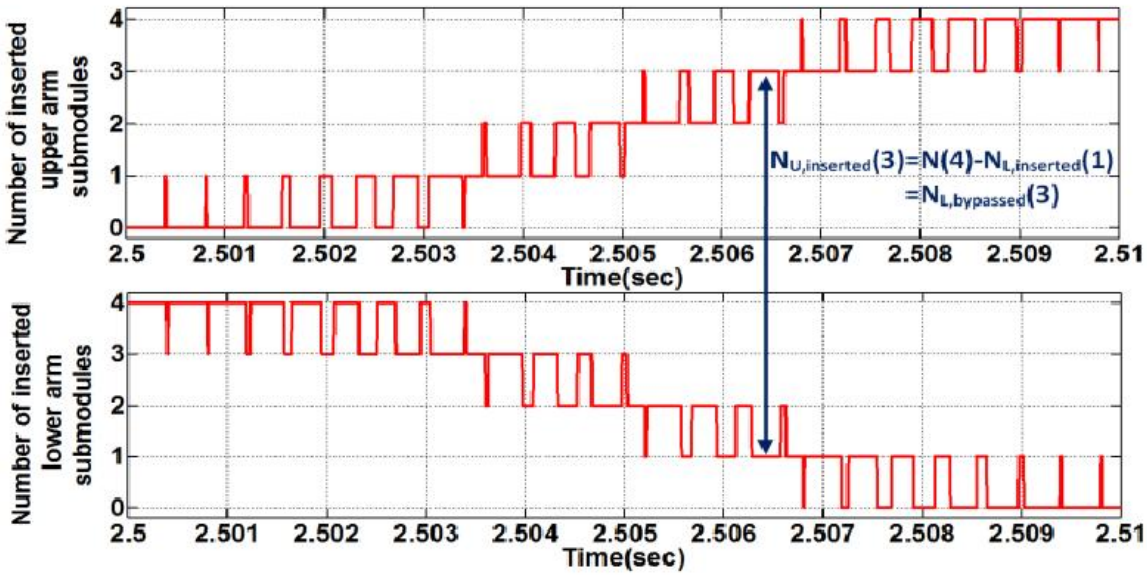

Figure6. Number of inserted submodules for upper and lower arms.

The selection of submodules, which is the next step, can be done based on capacitor voltage measurements delivered from the submodules. When the multivalve current direction is known, it can be predicted whether the capacitor will charge or discharge when inserted. This information is used to insert or bypass the submodules closest to the range limits and, in this way, keep the capacitors' voltages balanced. A positive current will charge the inserted capacitors, while a negative current will discharge the capacitors. That leads to the next step, which is called submodule selection.

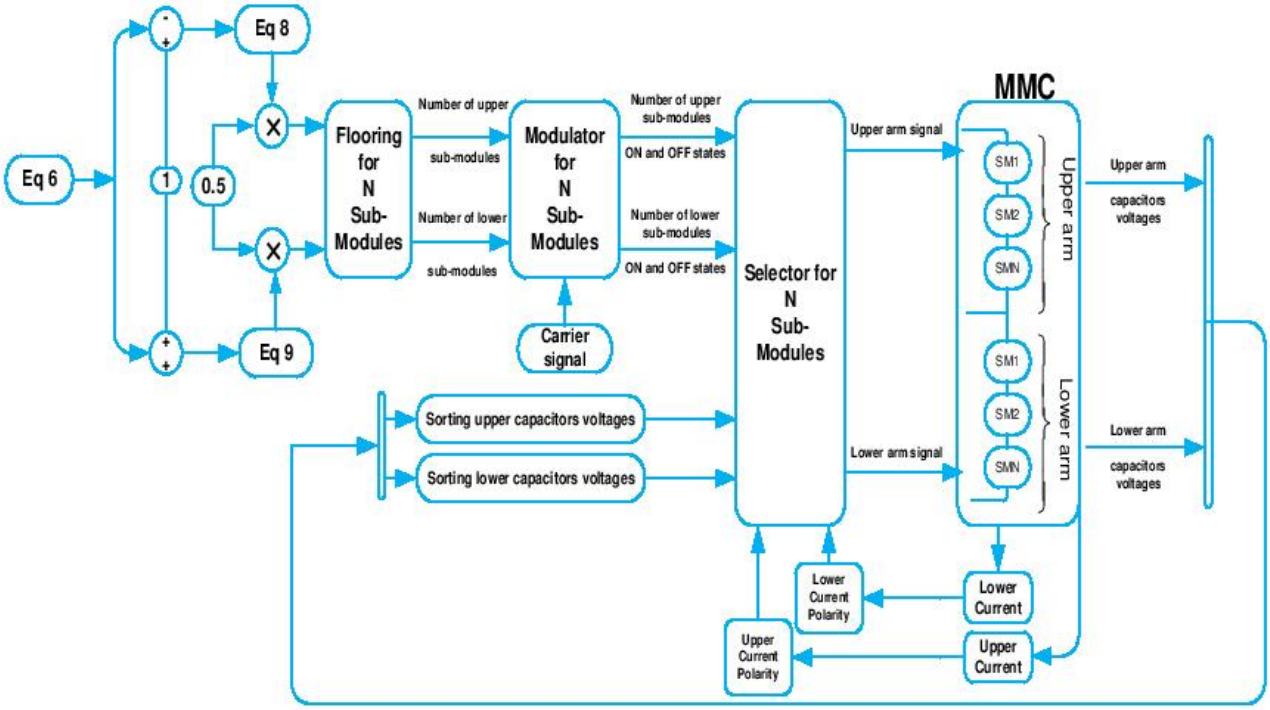

Figure 7. Proposed PWM algorithm with sorting voltage for MMC.

4. Submodules selection

To maintain the individual voltage of each submodule around its reference voltage takes an active balancing method. The voltage of each individual submodule together with the arm current needs to be measured and available in the voltage-balancing algorithm. The voltage-balancing algorithm selects the submodules in each of the arms of the converter based on the relative voltage values of all the arm submodules and direction of the arm current. Ascending or descending capacitor voltages are required to be used for balancing algorithm. The next submodule that switches in the arm is selected based on the direction of the current and the sorted voltages so that

- When the arm current is positive ($i_{arm} > 0$) and the modulation process method requires the addition of one submodule in the arm, the balancing algorithm will select the submodule with the lowest voltage that is not connected to be inserted into the arm.
- If the arm current is positive ($i_{arm} > 0$) and the modulation process method requires the subtraction of one submodule in the arm, the balancing algorithm will select the submodule with the highest voltage that is connected to the arm to be bypassed and removed from the arm.
- If the arm current is negative ($i_{arm} < 0$) and the modulation process method requires the addition of one submodule in the arm, the balancing algorithm will select the submodule with the highest voltage that is not connected to the arm to be inserted to the arm.
- If the arm current is negative ($i_{arm} < 0$) and the modulation process method requires the subtraction of one submodule in the arm, the balancing algorithm will select the submodule with the lowest voltage that is connected to the arm to be bypassed and removed from the arm.

The capacitor voltage of the submodule will not change when the submodule is not connected to the arm of the converter; it will remain at the level it was before it was removed from the arm of converter. The voltage balancing algorithm uses the data coming from the modulation process, upper and lower arms currents, and upper and lower arms sorting voltages. Figure7 shows the proposed PWM algorithm sorting both arms voltages. The main aim of the selection process is to maintain the voltages of the capacitors close to the reference values.

This is accomplished during the whole cycle of the waveform and the capacitors' actual voltages drift from their reference value within this cycle due to the load current coming from upper and lower arms currents. Moreover, the algorithm

considers the actual values for capacitor voltages coming from voltages measurements after sorting them in the selection of the submodules, but their relative voltage relates to the remaining submodules in the arm. In some cases, the submodule selected to be inserted into the arm of the converter according to the logic of the algorithm will further deviate from the reference voltage. The balancing of the submodule is not an instantaneous process and balancing around the reference occurs over the fundamental period.

IV. SIMULATION RESULTS

A number of simulations in MATLAB/Simulink have been verified through the operation of MMC under the proposed algorithm. The results for the 481-level in the output voltage waveform have been considered for the N+1 approach towards MMC using the proposed algorithm.

The case of the N+1 approach and a converter with 480 submodules per arm of the converter is considered to derive a waveform with an odd number of levels. To evaluate the proposed algorithm, time simulations were conducted on an MMC model. The ratings of the simulated converter are given in Table III.

The main idea is to prove that this proposed algorithm is very efficient, even though it is not based on any internal state measurements. Figs. 8 to 11 show the simulation results for the proposed algorithm. In Figure 8, the output voltage and current is purely sinusoidal.

TABLE III. SIMULATION PARAMETERS FOR THE N+1 MODULATION

Parameters	N+1 approach	Parameters	N+1 approach
DC bus	2200 kV	L_{arm}	1.25 H
R_{load}	160 Ω	Submodule voltage	5.5 kV
L_{load}	160 mH	R_{arm}	1.4 Ω
Module capacitance C	28.4 mF	Target capacitor voltage ripple	%5
Number of submodules per arm	480	Number of output levels	481
Load factor	0.95	Carrier frequency	1.5 kHz

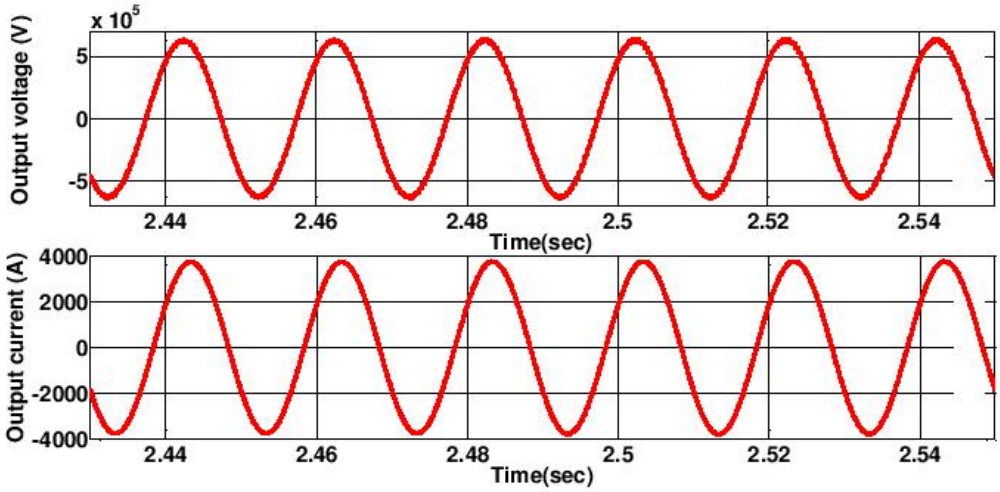

Figure 8. AC output phase voltage and current for MMC at 481 level by using the proposed control.

The arm currents, however, which are shown in Figure9, seem to contain very small second harmonic components. **Figure10 shows the intermediate capacitors' voltages for the both upper and lower arms. The target ripple for each** capacitor voltage (6%) had almost been achieved, at less than 7%. In addition, the circulating current I_{cir}, periodic with 10 ms cycle, had a small amplitude of about 60 A peak to peak, with ripple less than 9%, as shown in Figure11.

The FFT analysis for the arm currents and the output voltage of one phase leg were recorded. The arm current THD factor reached 1.6%. The output voltage THD factor reached 0.76%. Finally, the output current THD factor reached 0.26%. All

of the above indicate that the agreement between the use of the proposed algorithm for MMC and the required THD at the AC side to avoid using filters is rather satisfactory.

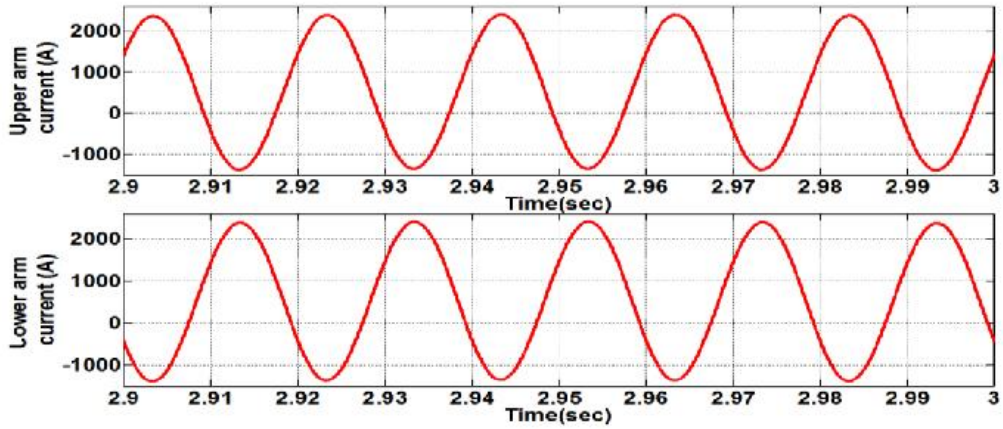

Figure 9. Upper and lower arms' currents for MMC at the 481 level by using proposed control.

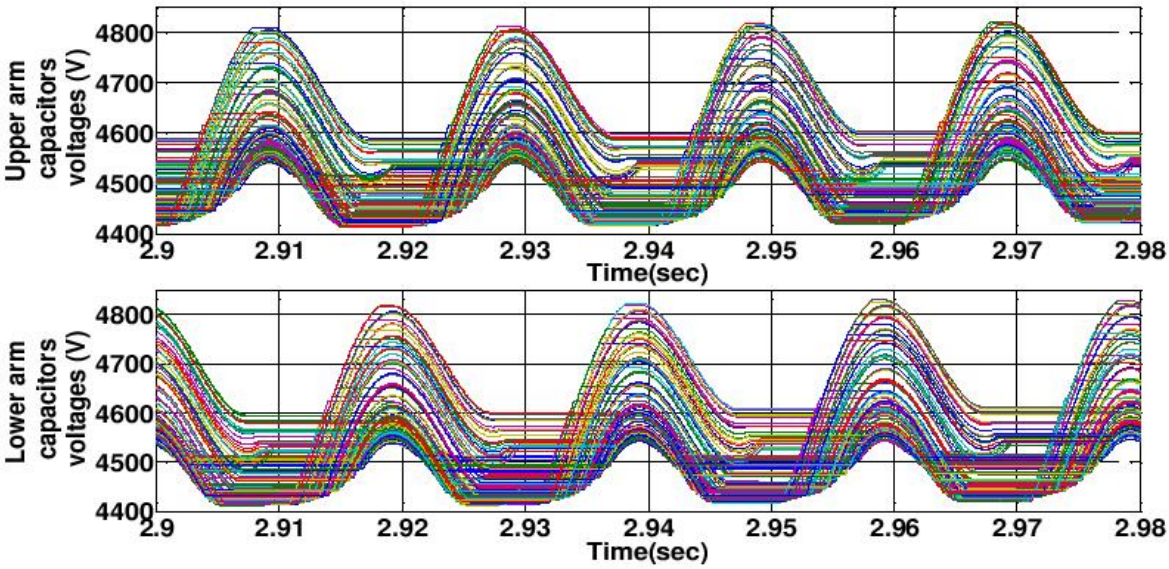

Figure 10. Upper and lower arms' intermediate capacitors' voltages for MMC at the 481 level by using the proposed control.

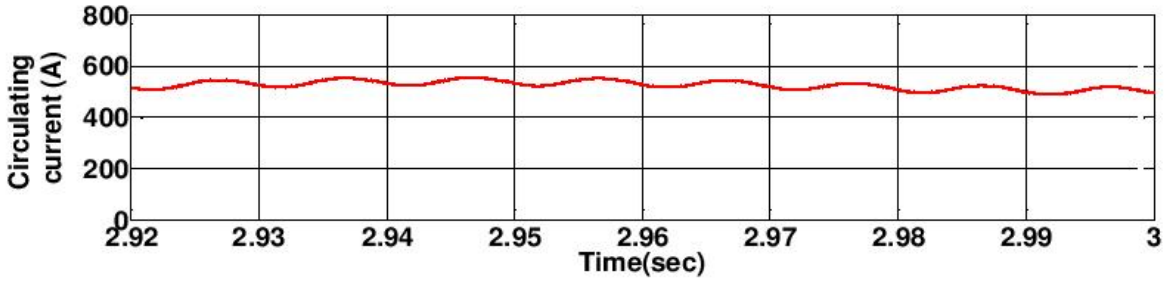

Figure 11. Circulating current for MMC at 481 level using the proposed control.

V. EXPERIMENTAL RESULTS

The proposed control for the MMC is also verified on a phase-leg experimental prototype with two submodules per arm as shown in Figure12. The proposed algorithm for the MMC was also verified on a phase leg experimental prototype with two submodules per arm. The specifications of the laboratory prototype are given in Table IV. The modulation and voltage sorting and balancing algorithms were implemented using the DSP F2812 board. The final form of a prototype MMC board is equipped with eight switches on a heat sink as depicted. Each submodule needs a blocking ability of about

200 to 275 volts. The proposed algorithm for the MMC was tested first as a final MMC control validation approach. The results, given below, correspond to a single-phase operation with 3 kHz switching frequency. Figure13 shows the output voltage of the 3-level modulation concept and output phase current. The voltage inside each level varies, as the capacitor voltages are not constant. Figure14 shows the result of upper and lower arms' currents (first and second from top to bottom) as described in (3) (which is given at the bottom of Figure14), giving the output current (fourth, from top to bottom) and the measured output current waveform (third from top to bottom). The upper arm current generates the positive half cycle for the AC output current, and the lower arm current generates its negative half cycle.

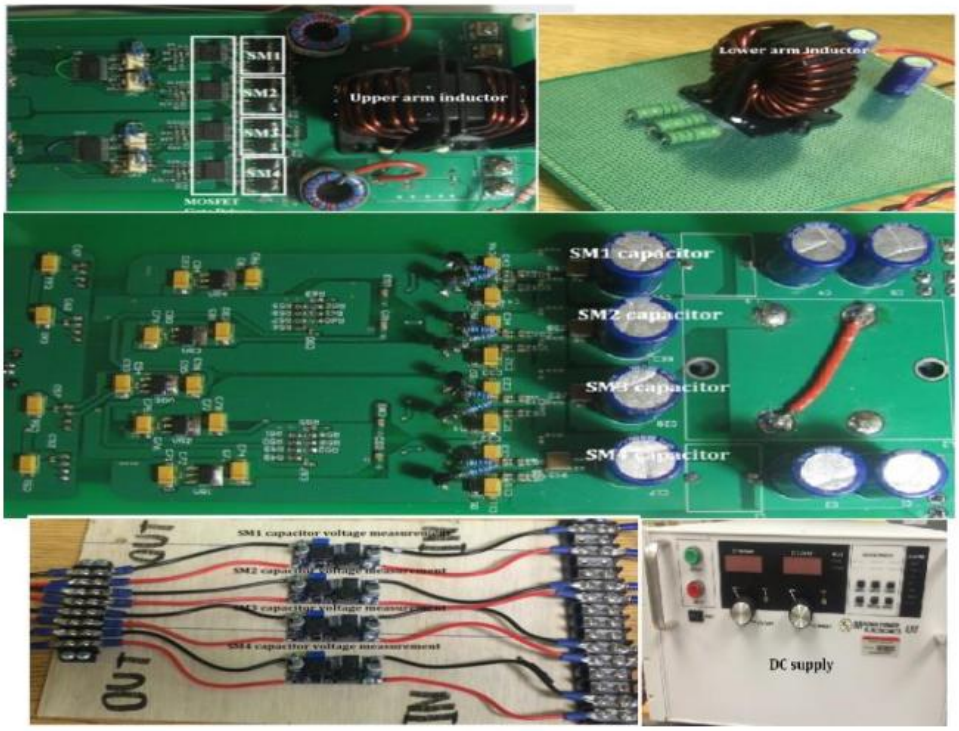

Figure 12. Laboratory prototype modular multilevel converter phase-leg

TABLE IV: MMC LABORATORY PROTOTYPE SPECIFICATIONS

Parameters	Values
DC voltage	500 V
R_{load}	20 Ω
L_{load}	2.2 mH
Submodule capacitance	2.2 mF
Arm inductance	3.5 mH
Arm resistance	0.1 Ω
Number of submodules per arm	2
Submodule voltage	250 V
Number of output level	3
Reference frequency	50Hz
Carrier frequency	3KHz

Figure15 shows the results of the upper (at top) and lower (at bottom) arms' voltages as described in (5) (which is given at the bottom of Figure15), giving the output voltage (at middle). Unlike the output current waveform, the upper arm voltage generates the negative half cycle for AC output voltage and lower arm voltage generates positive half cycle for AC output voltage.

The waveform circulating current, I_{cir}, of a 10 ms period, shown in Figure16, was as expected. Even thought dead time between two complimentary switches has an effect on the converter operation, and the small number of submodules per arm is used experimentally, The THD factor reduction proves the effectiveness of the controller in steady state, and since the whole design concept was based on the mathematical assumption that the circulating current consists only of a plain

DC component, the second order harmonic of the current has been eliminated. Compared to other types of control, peak-to-peak for the circulating current with two submodules reaches to %90 while in Figure16 is less than %35.

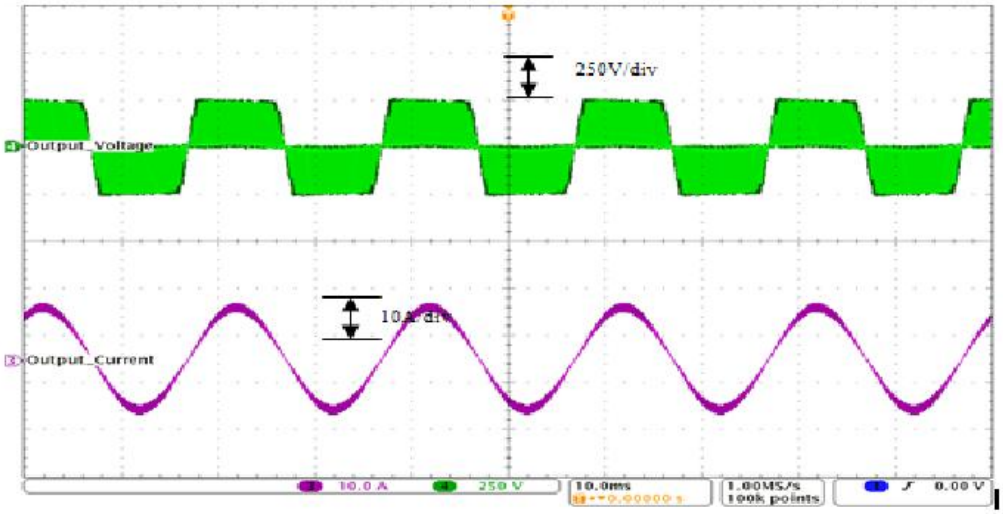

Figure 13. Experimental results: Three-level phase voltage and load current.

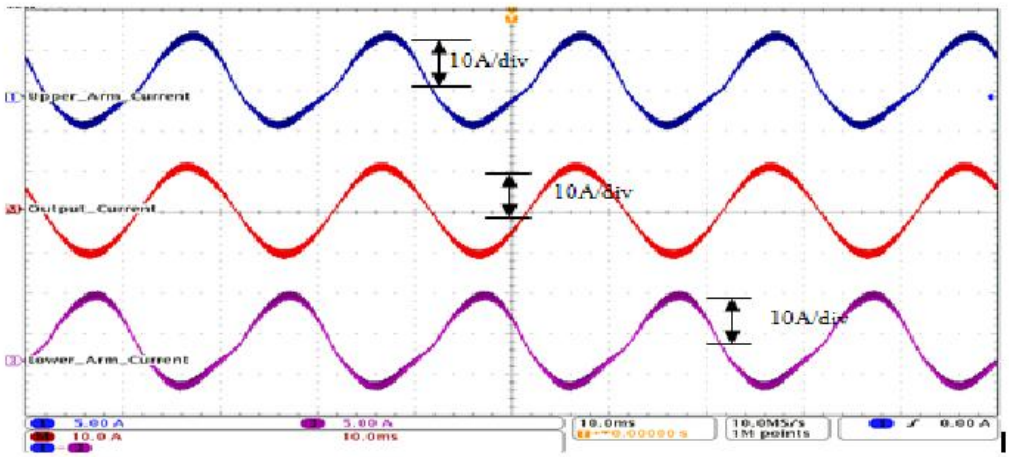

Figure 14. Experimental results: From top to bottom, upper arm current, lower arm current, and output current of MMC

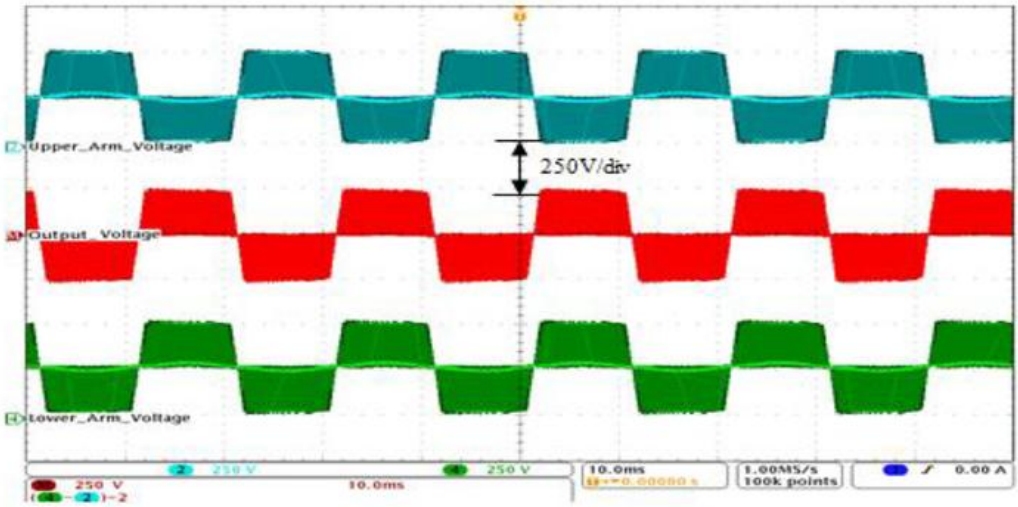

Figure 15. Experimental results: Upper arm voltage (top), lower arm voltage (bottom), and output voltage (middle) of the MMC.

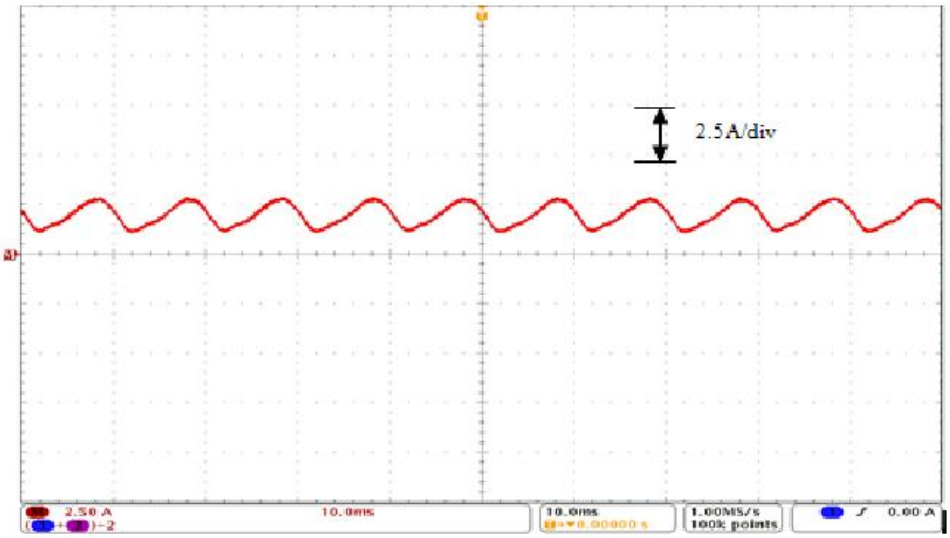

Figure 16. Experimental results: Circulating current through the circuit of the MMC.

VI. CONCLUSION

In this paper, the arms' voltage and energy equations were derived and presented, describing the main idea of MMC act in single phase. Introducing a new topology for MMC with a large number of output voltage levels based on arm energy approximation control has been proposed in order to use it with a wide range number of submodules which can be used for high- and extra-rate power applications. Generating insertion indices, which are considered the starting point for the proposed algorithm for number of submodule per arm (N), were derived. The proposed PWM control comes to fulfill the requirements of UHVDC bus voltage in this paper with many contributions. Since there will be demand for UHVDC in the next years (2200 kV and more) The paper proposes MMC topology with more submodules per arm to achieve large scale of output voltage levels based on simple algorithm control. Also, Since the number of submodules is hundreds in UHVDC, sinusoidal AC voltage waveforms will be achieved and THD will be limited to less than one to avoid using AC filters. The proposed method works with low switching frequency for UHVDC systems, which will decrease converter losses. Moreover, for MMC itself the proposed method offers simple numerical algorithm for MMC topology that can be used with large or small number of submodules per arm either experimentally or by simulation. Selection process for inserting or bypassing submodules guarantees capacitors voltages around the reference voltage (Vdc/N) with voltage ripple less than 7% even for large number of submodules per arm. More converter stability can be achieved by equal sharing of currents from both arms to the load. Overall, the proposed PWM allows MMC to be used with large scale of power transmission either HVDC systems or large scale of solar energy and also can be used for large motors control. The theoretical analysis has been verified through extended simulation results with 481 level and experimentally on a laboratory prototype phase leg of the MMC with four submodules based on arm energy approximation control.

REFERENCES

[1] A. Lesnicar, R. C. Marquadt., "A new modular voltage source inverter topology," Institute of Power Electronics and Control, Universität der Bundeswehr München, Werner-Heisenberg-Weg 39, 85577 München, Germany, 2004.

[2] A. Das, H. Nademi and L. Norum, "A Method for Charging and Discharging Capacitors in Modular Multilevel Converter," IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society, vol. 22, no. 5, pp. 1534-1545, Oct. 2010.

[3] H. Mohammadi and M. Tavakoli Bina, "A Transformerless Medium-Voltage STATCOM Topology Based on Extended Modular Multilevel Converters," IEEE Transaction on Power Electronics, ISSN 1553-572x, pp. 1058–1062, Nov. 2011.

[4] H. Fehr, A. Gensior and M. Muller, "Analysis and Trajectory Tracking Control of a Modular Multilevel Converter," IEEE Transaction on Power Electronics, vol. 30, no. 1, pp. 398–407, Jan. 2014.

[5] M. Zygmanowski, B. Grzesik, Marek Fulczyk and Radosław Nalepa, "Analytical and Numerical Power Loss Analysis in Modular Multilevel Converter," Ind. Electron. Society, IECON 2013 - 39th Annual Conference of the IEEE., ISSN 1553-572x, pp. 465–470, Nov. 2013.

[6] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2MWpower rating and 17-level-output-voltage," in Power Electronics. Specialist Conf., PESC, pp. 2572–2576, 2004.

[7] H. Akagi, "Classification, terminology and application of the modular multilevel cascade converter (MMCC)," IEEE Transaction on Power Electronics., vol. 26, no. 11, pp. 3119– 3130, 2011.

[8] S. Deore, P. Darji and A. Kulkarni, "Switching function analysis of half- and full-bridge modular multi-level converters for HVDC applications," Generation, Transmission & Distribution, IET, vol. 7, no. 11, pp. 1344–1365, Nov. 2013.

[9] C. Wang, Q. Hao and B. Ooi, "Reduction of low-frequency harmonics in modular multilevel converters (MMCs) by harmonic function analysis," Generation, Transmission & Distribution, IET, vol. 8, no. 2, pp. 328–338, Feb. 2014.

[10] E. Abildgaarda and M. Molinas, "Modelling and Control of the Modular Multilevel Converter (MMC),. Technoport 2012 - Sharing Possibilities and 2nd Renewable Energy Research Conference (RERC2012), vol. 20, pp. 227–236, 2012.

[11] X. Lia, Q. Songa, W. Liua, Q. Lia, H. Raob and S. Xu, "Zero-sequence voltage injection control scheme of modular multilevel converter supplying passive networks under unbalancedload conditions," Electric. Power System Research., Nov. 2011.

[12] L. Harnefors, A. Antonopoulos, S. Norrga, L. Ängquist, and H. Nee, "Dynamic Analysis of Modular Multilevel Converters," IEEE Transactions on Industrial Electronics, vol. 60, no. 7, pp. 2526–2537, Jul. 2013.

[13] Abd Almula Gebreel, and Longya Xu, "DC-AC Power Conversion Based on Using Modular Multilevel Converter With Arm Energy Approximation Control," IEEE Power and Energy Technology Systems Journal, Vol:PP , No 99 , pp. 1–11, Feb. 2016.

[14] D. Siemaszko, "Fast Sorting Method for Balancing Capacitor Voltages in Modular Multilevel Converters," IEEE Transaction on Power Electronics, vol. 30, no. 1, pp. 463–470, Mar. 2014.

[15] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," IEEE Transaction on Power Delivery, vol. 25, no. 4, pp. 2903-2912, 2010.

[16] J. Pou, S. Ceballos, G. Konstantinou, V. Agelidis, R. Picas, and J. Zaragoza, "Circulating Current Injection Methods Based on Instantaneous Information for the Modular Multilevel Converter," IEEE Transaction on Industrial Electronics vol. pp 1-11, no. 99, pp. 1, Jul. 2014.

[17] Abd Almula Gebreel, , Longya Xu, "Power quality and total harmonic distortion response for MMC with increasing arm inductance based on closed loop-needless PID controller," Electric Power Systems Research, Vol. 133, Apr. 2016, Pages 281–291.

[18] Abd Almula Gebreel, "Numerical Analysis and Simulation Implementation for SVPWM Based on a New Region Segment Configuration Method," International Journal of Scientific and Engineering Research, Vol. 6, No. 3, pp. 614–621, March 2015.

[19] H. Bärnklau, A. Gensior and J. Rudolph, "A Model-Based Control Scheme for Modular Multilevel Converters," IEEE Transactions on Industrial Electronics, vol. 60, no. 12, Dec. 2013.

[20] K. Ilves, A. Antonopoulos, S. Norrga and H. Nee, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," IEEE Transaction on Power Electronics vol. 27, no. 1, pp. 57–68, Jun. 2012.

[21] Abd Almula Gebreel, "Survey on Topologies, and Control Techniques for the Most common Multilevel Inverters," International Journal of Scientific and Engineering Research, Vol6 6, No. 6, pp. 614–621, June 2015.

[22] M. Guan, and Z. Xu , "Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions," IEEE Transaction on Power Electronics vol. 27, no. 12, pp. 4858–4867, Dec. 2012.

[23] A. Antonopoulos, L. Angquist and H. Nee, "On dynamics and voltage control of the modular multilevel converter," Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, pp. 1–10, Sep. 2009.

[24] G. Konstantinou, M. Ciobotaru and V. Agelidis, "Operation of a modular multilevel converter with selective harmonic elimination PWM," Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on, pp. 999–1004, Jun. 2011.

[25] K. Ilves, A. Antonopoulos, S. Norrga and H. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," IEEE Transactions on Power Electronics, vol. 27, no. 8, pp. 3482–3494, Jan. 2012.

[26] A. Antonopoulos, K. Ilves, L. Angquist, H. Nee, "On interaction between internal converter dynamics and current control of high-performance high-power AC motor drives with modular multilevel converters" Energy Conversion Congress and Exposition (ECCE), pp. 4293–4298, Sep. 2010.

[27] G. Konstantinou, M. Ciobotaru and V. Agelidis, "Analysis of multi-carrier PWM Methods for back-to-back HVDC systems based on modular multilevel converters," IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society, pp. 4238–4243, Nov. 2011.

[28] N. Ahmed, A. Haider, D. Hertem, L. Zhang and H. Nee, "Prospects and challenges of future HVDC super-grids with modular multilevel converters," Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, pp. 1–10, Sep. 2011.

[29] X.Yang, C. Zhao, J. Hu, J. Wang, and L. Yang , "Key technologies of three-terminal DC transmission system based on modular multilevel converter," Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011 4th International Conference on, pp. 499–503, Jul. 2011.

[30] Q. Tu and Z. Xu, "Power losses evaluation for modular multilevel converter with junction temperature feedback," Power and Energy Society General Meeting, 2011 IEEE, pp. 1–7, Jul. 2011.

[31] T. Modeer, H. Nee and S. Norrga, "Loss comparison of different sub-module implementations for modular multilevel converters in HVDC applications," Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference, pp. 1–10, Sep. 2011.

[32] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," IEEE Transaction on Power Delivery, vol. 26, no. 1, pp. 298–306, 2011.

[33] Z. Li, Y. Li, P. Wang, H. Zhu, Z. Chu and S. Wang, "Improving the performance of modular multilevel converter by reducing the dead time effect," Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference, pp. 1–10, Sep. 2011.

[34] M. Tomasini, R. Feldman, J. Clare, P. Wheeler, D. Trainer and R. Whitehouse, "DC-Link voltage ripple minimization in a modular multilevel voltage source converter for HVDC power transmission," Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference, pp. 1–10, Sep. 2011.

[35] S. Fan, K. Zhang, J. Xiong, and Y. Xue , "An Improved Control System for Modular Multilevel Converters with New Modulation Strategy and Voltage Balancing Control," IEEE Transaction on Power Electronics, vol. 30, no. 1, pp. 358–371, Jan. 2015.

[36] Y. Zhang, G. Adam, T. Lim, S. Finney, and B. Williams, "Mathematical Analysis and Experiment Validation of Modular Multilevel Converters," Journal of Power Electronics, vol. 12, no. 1, pp. 33-39, 2012.

[37] Y. Zhang, G. Adam, T. Lim, S. Finney, and B. Williams, "Parameter Design Principle of the Arm Inductor in Modular Multilevel Converter based HVDC," Power System Technology (POWERCON), 2010 International Conference, pp. 1–6, 2010.

[38] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and Inductance Selection of the Modular Multilevel Converter," Power Electronics and Applications (EPE), 2013 15th European Conference, pp. 1–10, Sep. 2013.

[39] D. Melvold and W. Long, "Back-to-Back HVDC System Performance with Different Smoothing Reactors," IEEE Transaction on Power Delivery, vol. 4, no. 1, pp. 208–215, Jan. 1989.

[40] D. Melvold and H. Lips, "Effects of Operating Configurations of Multi-Terminal HVDC Systems on DC Filter Performance," IEEE Transaction on Power Delivery, vol. PWRD-2, no. 3, pp. 924–930, Jul. 1987.

[41] H. Bawa, "ABB develops complete system solution for 1,100 kV HVDC power transmission." [Online]. Available: http://www.abb.com/cawp/seitp202/3a8302e9925218a4c1257d3f00451b52.aspx

[42] State Grid: Corporation of China, "Technology Specifications for ±1100 kV UHV DC Power Transmission Equipment Research Published." [Online]. Available: http://www.sgcc.com.cn/ywlm/mediacenter/corporatenews/05/247215.shtml

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